OK Cantrell 04/24/07

REMARKS

I. STATUS OF CLAIMS

In accordance with 37 C.F.R. § 1.173(c), the status of the claims are as follows:

Claims 1-33 and 40-54 are pending in the reissue application.

Claims 1-33 are original claims and remain allowed. No changes have been made to claims 1-33.

Claims 34-54 were previously added in the preliminary amendment filed November 24, 2003, with claims 34-39 being canceled in the previous amendment filed November 20, 2006.

No amendments are being made in this response.

II. PRIOR ART REJECTION

Claims 34-54 stand rejected under 35 U.S.C. § 102 as being anticipated by Eickemeyer et al. '746 ("Eickemeyer"). Claims 40 and 47 are independent. This rejection is respectfully traversed for the following reasons.

Claims 40 and 47 each embody an instruction bus formed between the instruction supplying/issuing unit and the decoding unit, wherein the bit width of the instruction bus is shorter than M * N bits; where M is the maximum bit length of an instruction that can be executed in parallel and N is the number of instructions that can be executed in parallel. In direct contrast, Eickemeyer expressly discloses (col. 12, lines 5-14):

> the rule for compounding a set of instructions which includes variable instruction lengths provides that all instructions which are 2 bytes or 4 bytes long are compoundable with each other. That is, ... a 4 byte instruction is capable of parallel execution with another 2 byte ***or another 4 byte instruction***. The rule further provides that all instructions which are 6 bytes long are not compoundable. (emphasis added)